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Ultrafast Integrated Optical Signal Processing

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Final Report

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Massachusetts Institute of Technology
January 28, 2010

We investigated the fabrication and optical characterization of a photonic integrated circuit (PIC) designed for telecommunication applications using ultrafast (> 100Gbits/s) optical logic. The basic components in the PIC are active components, such as semiconductor optical amplifiers (SOAs), integrated with passive, light-routing waveguides and beam splitter/combiners. Optical switching is accomplished with SOAs embedded within the arms of Mach-Zehnder interferometers (MZIs), whereas power splitting/combining of propagating signals is carried out within multimode interferometers (MMIs). Figure 1 shows a schematic of the basic unit cell under investigation.
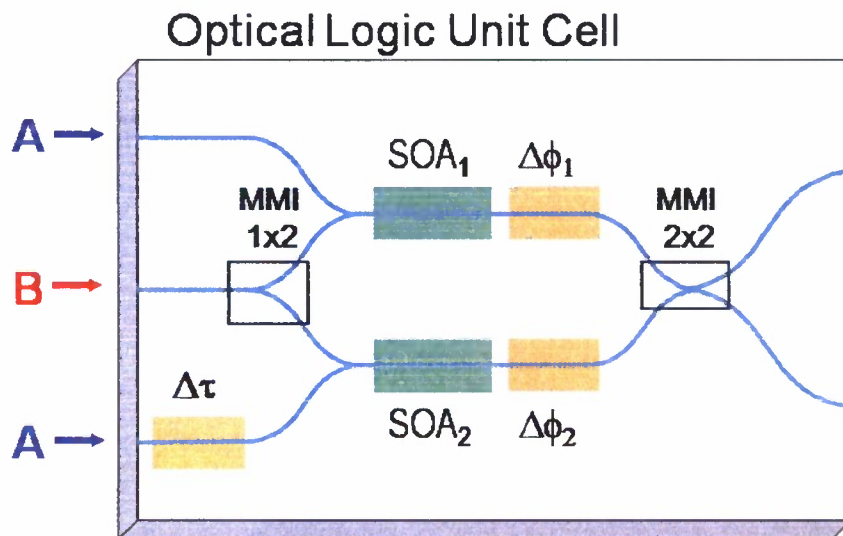

Figure 1: Schematic drawing of a unit cell that represents the heart of the photonic integrated circuit under investigation. A and B are to represent different wavelengths of input signals. Four amplifiers are shown; two are used to bias the two arms of the interferometer (SOA$_1$ and SOA$_2$), and two are for adding a phase shift to the propagating signals ($\Delta\Phi_1$, $\Delta\Phi_2$). (A time delay element, $\Delta\tau$, is also illustrated, but was not investigated here.)

In this investigation, the method for integrating the active components, SOAs, with the passive components, waveguides and MMIs, involved the use of an asymmetric twin-waveguide approach pioneered by Studenkov, *et al.* [1-4]. Such a monolithic integration approach vertically

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couples an active and passive waveguide together allowing optical mode transfer between them. In order to couple between the active and passive waveguides, an adiabatic taper is used [4]. By slowly varying the width of the active waveguide along the taper, the effective index will also slowly change. At a particular width, the active and passive waveguides will be locally symmetric, have matching effective indices, and a strong local resonance will exist between the two modes. Therefore, there will be strong coupling and optical power will be transferred from one mode to the other moving the signal between the passive waveguide and the active amplifier portion of the PIC. The end width of the taper is sufficiently small, less than 1 μm, to ensure that the taper's effective guiding index is insignificant, to minimize any reflections, and to maximize coupling. The entire structure is grown epitaxially as a single heterostructure, and the devices can be fabricated using standard planar fabrication techniques. The benefits available when integrating using the asymmetric twin-waveguide approach includes the elimination of any re-growth steps, and focuses on creating the integrated circuit with planar processing techniques. Below, in Figure 2, is a cross-sectional schematic of the SOA integrated with the passive waveguide highlighting the key processing steps including: epitaxy of passive and active semiconductor layers, pattern definition with photolithography and inductively-coupled reactive ion etching of the III-V semiconductors, planarization of the circuit using benzocyclobutene (BCB) and metallization of the top and bottom contacts. [Note: a portion of the BCB passivation layer is removed to illustrate the passive/active coupling with the taper.] The taper length was chosen to be 175 μm, with optical power transfer at that length modeled to be approximately 96%. Multimode interferometers were simulated and designed for 1x2 and 2x2 configurations. Using guided-mode propagation analysis and BPM simulations [5] at 1550nm, the optimized dimensions for the 1x2 MMI were determined to be 159 μm long and 12 μm wide. The optimum 2x2 MMI dimensions were determined to be 480 μm long and 18 μm wide.
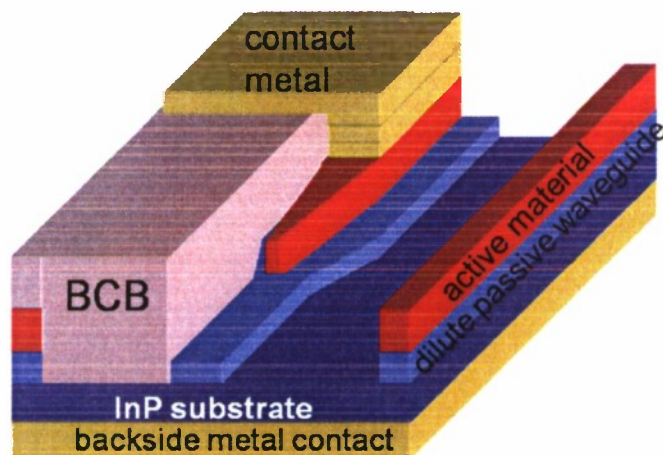

Figure 2: Cross-sectional schematic of the PIC emphasizing the passive waveguide to active semiconductor optical amplifier integration.

The epitaxial layers were designed with the beam propagation method (BPM), using the software program RSoft BeamPROP (Version 5.0) for calculations [5]. Figure 3 shows the cross-section of the heterostructure where a dilute waveguide was implemented for the passive guiding layer. $In_{0.8}Ga_{0.2}As_{0.45}P_{0.55}$ with a characteristic wavelength of 1180nm was clad with InP. The design was optimized for a ridge waveguide that is 4 μm wide and 1.05 μm tall. The active portion of

the epitaxial structure was a double heterostructure configuration with a 200 nm thick $In_{0.56}Ga_{0.44}As_{0.94}P_{0.06}$ quaternary layer emitting at 1550nm in order to amplify the incident data pulse. The epitaxial structure was grown using metalorganic chemical vapor deposition (MOCVD) and was purchased from IQE, Inc.
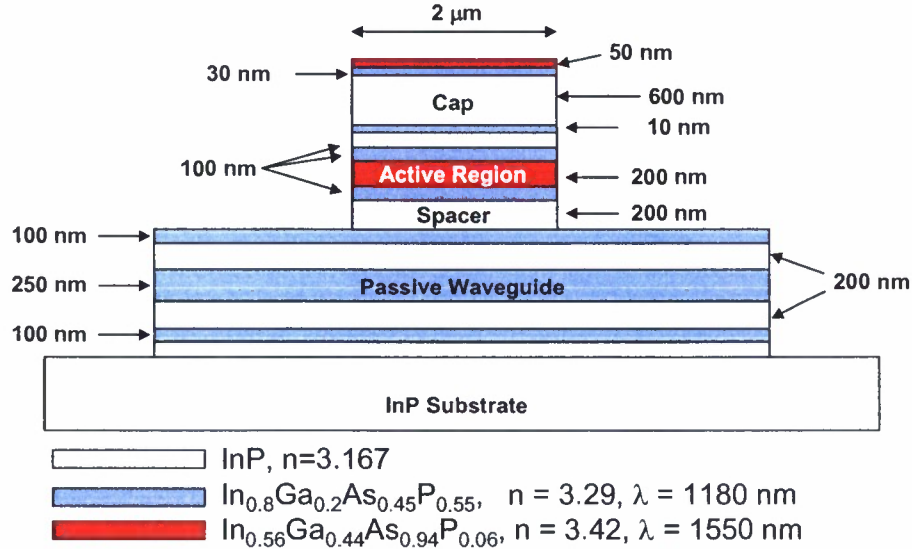

Figure 3: Schematic of the epitaxial heterostructure designed for the asymmetric twin waveguide passive/active coupling scheme.

After the III-V semiconductor layers are etched, additional fabrication steps are required to planarize the PIC and prepare the devices for metallization, lapping and cleave. Figure 4 shows a scanning electron micrograph (SEM) of the reactive-ion-etched III-V layers [6].
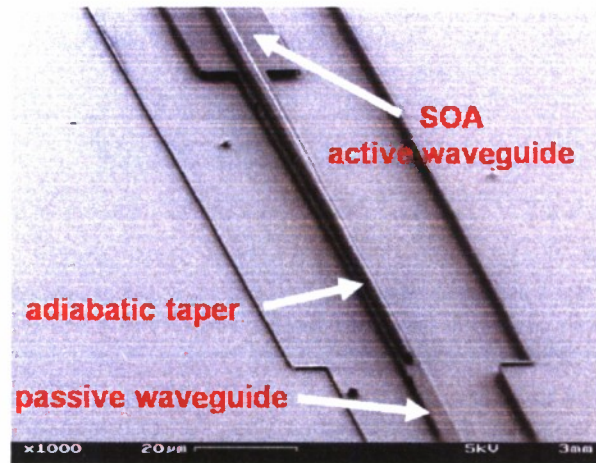

Figure 4: Scanning electron microscope image of the fabricated twin waveguide structure etched in the InP/InGaAsP semiconductor material. The devices are placed within a trench to minimize the volume of III-V material etched and improve etch reproducibility.

It is important to note that the total etch depth to define the underlying passive waveguide requires approximately 2.4 μm of material to be removed; additionally, the resultant etched III-V wafer contains significant wafer topology that subsequently must be planarized. The process optimized for planarization utilized BCB. Initially the BCB process was problematic as sidewall adherence of the BCB to the etched III-V waveguide was insufficient, as seen in the top left panel of Figure 5. Moreover, several different BCB formulations were examined with various viscosity and layer thickness to determine the proper formulation that was necessary to completely and fully achieve planarization of the PIC with significant surface topology. The bottom panel of Figure 5 shows the scanning electron micrograph of a successfully planarized test wafer used to optimize the process flow.
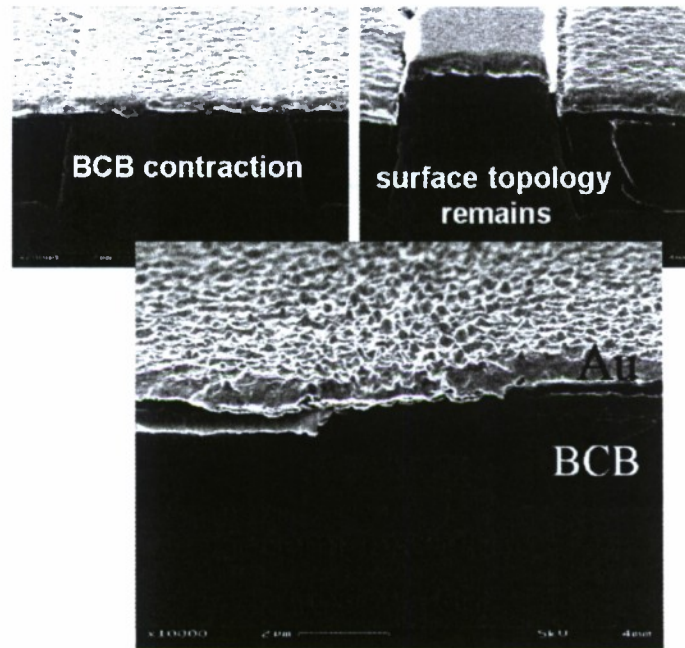

Figure 5: Cross-sectional SEM images showing the issues with the benzocyclobutene (BCB) planarization layer and the Ti/Pt/Au ohmic contact. The top active ridge is 4 μm wide. Top left panel shows the issues related to BCB contraction away from the sidewall of the etched waveguide, whereas top right panel show insufficient addition of BCB such that full and complete planarization was not achieved. The bottom panel shows a test wafer with proper BCB planarization followed by metallization.

Following planarization of the PIC, the BCB is etched back with reactive ion etching to expose the SOA surface requiring metallization. Originally, approximately 300nm of metal was applied to the top p-type doped contact layer of the SOA. However, subsequent electrical probing with a metal tip proved to be destructive to the SOA metal contact and ultimately resulted in an open circuit and even complete removal of the metal layer. Two solutions were found: (i) the top metal contact layer was increased to 1 μm by carrying out multiple metallization steps, and (ii) gold electroplating was used for the final top-side metallization scheme. Figure 6 shows a microscope image of the top of the PIC after electroplating was used for the metallization process. The electroplating metallization process easily allowed for the deposition of over 2 μm

of gold metal and greatly enhanced the ability to carry out electrical testing. The top p-type contact layer of semiconductor was doped at $2x10^{18}$ cm^{-3} and resulted in a relatively large contact resistance of near 10^{-4} Ω cm^2. Such large contact resistance also resulted in large ohmic drops across the diodes. Wafers were therefore ion-implanted and annealed to decrease the contact resistance to $3x10^{-6}$ Ω cm^2.
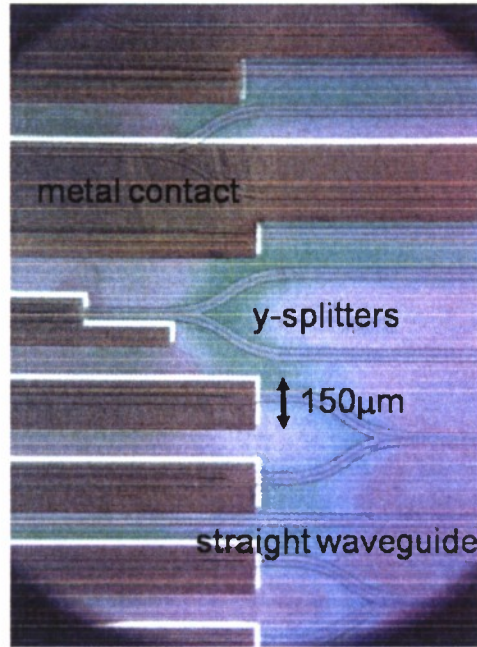

Figure 6: Microscope image of the top-side of the PIC showing the metal contacts formed by gold electroplating; the contact layer is approximately 2.4 μm thick. Here the y-splitters are easily seen along with straight waveguides.

The photonic integrated circuit was composed of a number of devices including straight passive waveguides, MMI power splitters and combiners, Mach Zehnder interferometers with SOAs in the arms, as well as the full unit cell seen in the schematic of Figure 1. Figure 7 below shows the mask layout with the many device configurations; the left panel is the mask layout for the full die whereas the right panel is a closer view of various devices available for optical and electrical testing. Figure 8 shows a photograph of the mounted PIC ready for characterization. Optical characterization was carried out on the passive components as well as the PIC. Power splitting in the MMIs was observed by viewing the output of a 1x2 MMI power splitter at the facet of the photonic integrated circuit The optical signal is seen to be split 50:50 between the two output arms. Loss measurements were carried out on the straight passive waveguides that were composed of the dilute quaternary InGaAsP interspersed between layers of InP (see epilayer schematic in Fig. 3). The data show that the waveguide loss was very low, 0.89 dB/cm, indicating that the fabrication of the passive waveguides was successful. In addition, some waveguides contained varying numbers of s-bends and relatively low loss was determined for these passive devices as well.
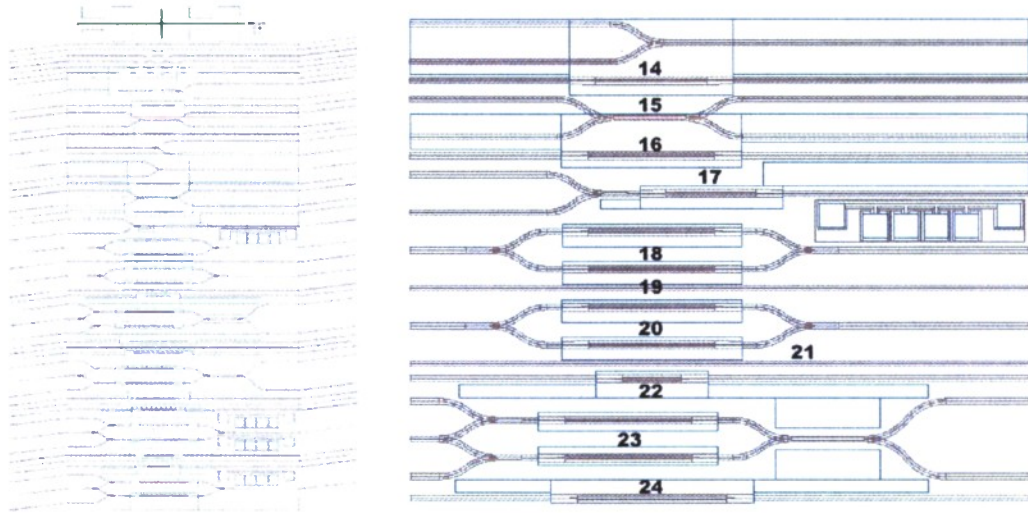
Figure 7: left panel shows the full mask layout for a single die as part of the photonic integrated circuit, right panel shows a closer view of all mask levels overlaid together. The boxes indicated the regions of metallization for electrical probing of the amplifiers. The MZIs are easily seen as well as the y-splitters and combiners.

Each quarter wafer processed has sufficient area for the production of 7 individual die, as seen in Figure 7, left panel. Individual SOAs were electrically biased during the propagation of optical signals to assess the degree of active/passive coupling and the amount of amplification that was provided by the SOAs. Coupling of amplified spontaneous emission into the underlying passive waveguide was seen when the SOAs were electrically biased. Figure 9 shows the spectrum for current levels of 100, 200, 300 and 400mA injected into the SOAs. Effective coupling of the light from the biased amplifier to the underlying passive waveguide was determined from these measurements.
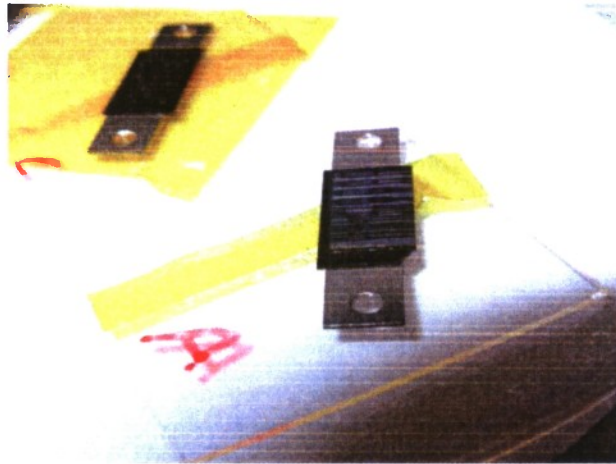

Figure 8: After metallization, each quarter wafer is lapped down to a thickness of 175μm, backside metal is evaporated, individual die are cleaved, and then the chips are mounted for electrical and optical testing. Photograph of the completed PIC is seen here.
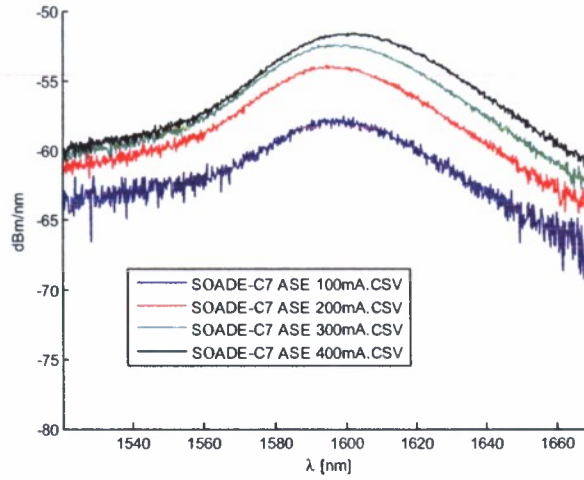
Figure 9: Amplified spontaneous emission (ASE) measured from a cleaved passive waveguide illustrating that electrically-pumped SOAs emit light and the asymmetric twin waveguide integration approach successfully couples light out of the amplifier. The device number is 24 as seen in Figure 7 right panel; the active region is 2μm wide and 1000μm long.

Optical characterization was also carried out on other dies containing similar passive/active integrated devices. As one may expect, some devices perform better than others since quarter wafers were processed throughout the entire 5 mask level process flow. In Figure 10 the optical output of a passive waveguide was measured as the current injected into an integrated active region was increased from 100mA to 400 mA. Clearly light is being generated in the active region, coupled effectively into the underlying passive waveguide and then guided with low loss to the cleaved output facet; laser oscillations are clearly observed indicating optical gain is achieved in the active material.
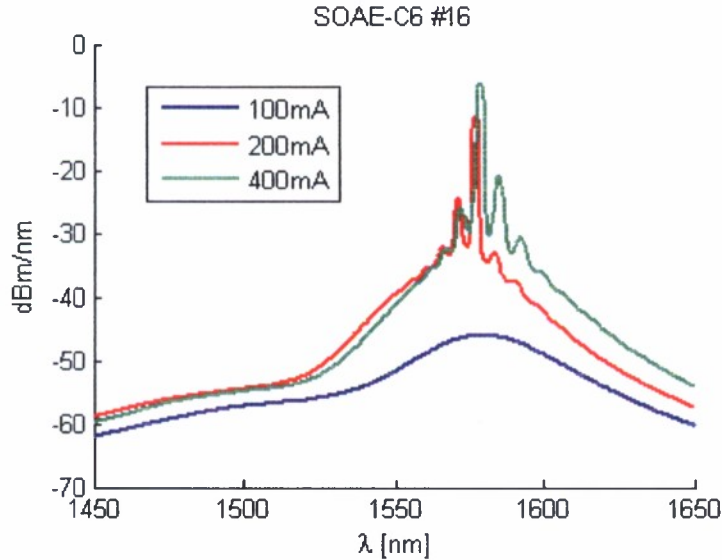

Figure 10: Optical spectrum recorded from the output of a straight passive waveguide containing a single SOA active layer and integrated with the asymmetric twin waveguide approach. The device number is 16 as seen in Figure 7, right panel; the gain region is 4μm wide and 850μm long.

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As seen in the mask layout in Figure 7, dozens of devices have been fabricated on numerous die and many different chips. Optical and electrical testing is being conducted on all of the many available devices and is in process currently.

Additionally, and in parallel, quantum dot materials emitting at 1550nm have been grown on InP substrates using molecular beam epitaxy. Although the current PIC contains a bulk active layer, ultimately, for ultrafast optical logic performance, quantum dot active layers will be required. A number of quantum dot structures have been grown and characterized. Epitaxial structures, grown in preparation for atomic force microscope characterization of the dots resting on the wetting layers, have quantum dot densities ranging from 3 to 70 per μm^2. Similarly, additional structures that are grown with the quantum dot layers capped appropriately for photoluminescence measurements show emission near the target wavelength of 1550nm; Figure 11 shows the room temperature photoluminescence emitted from one such test structure. As expected, the emission is quite broad indicating a range of dot sizes, but also the emission is quite strong.
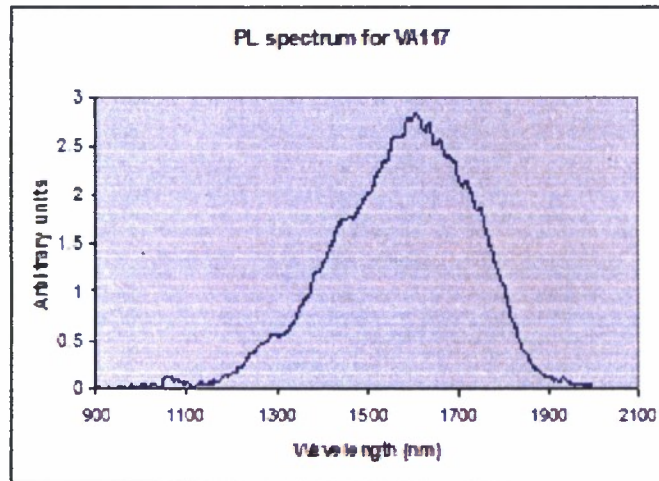

Figure 11: Photoluminescence at room temperature from InAs quantum dots embedded in a wetting layer of $In_{0.53}Ga_{0.36}Al_{0.11}As$, clad by $In_{0.8}Ga_{0.2}As_{0.45}P_{0.55}$.

To investigate the gain characteristics of the quantum dot material, laser structures were designed and grown by molecular beam epitaxy. Figure 12 shows the final laser heterostructure. The modulated sides of the schematic illustrate the approximate energy band alignment for the various layers such as quantum dot layer (InAs dots), wetting layer ($In_{0.53}Ga_{0.36}Al_{0.11}As$), cladding layer ($In_{0.8}Ga_{0.2}As_{0.45}P_{0.55}$) and optical confining layers (primarily InP). We have processed the quantum dot laser structure into buried ridge laser bars of varying width and length. Unfortunately we have been unable to measure any laser characteristics, although diode behavior was observed with a turn-on voltage near 0.7V. In collaboration with Thorlabs Quantum Electronics we are sending our quantum dot epitaxial material to Covega for laser manufacturing using their facilities; they also have not observed lasing from the quantum dot material. We believe two problems may be contributing to the inability to observe gain in the structures. Firstly, the quantum dot density may not be sufficient or the number of quantum dot layers should be increased. Secondly, the top p-type cladding and optical confinement layer may need

to be increased to greater than 2µm. We will continue our growth of quantum dot materials and the pursuit of quantum dot lasers. Ultimately our goal is to replace the bulk gain material in the SOAs of the PIC with quantum dot active material.
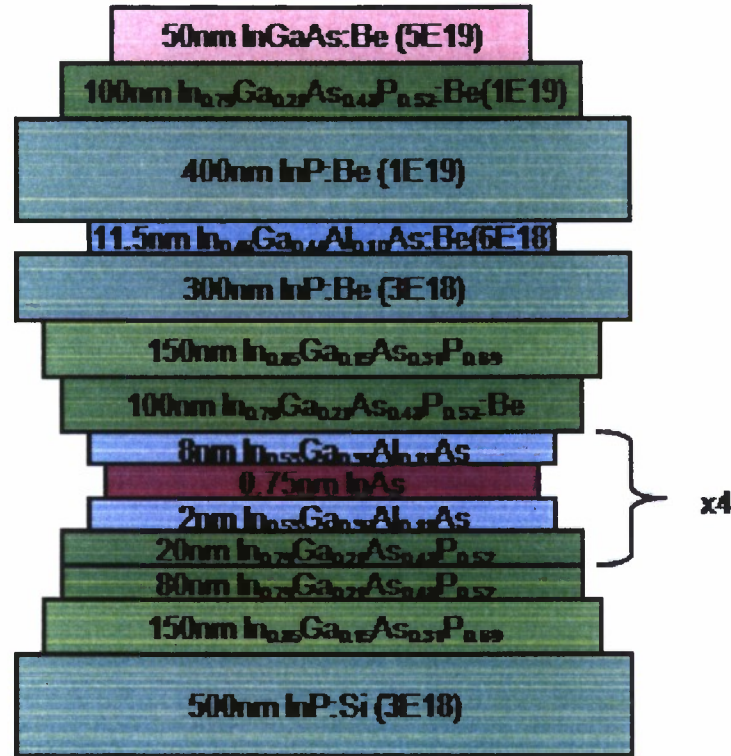

Figure 12: Schematic layer structure of the quantum dot laser. The InAs quantum dot layers are repeated four times.

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Re: Erich Ippen
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To Whom It May Concern:

Attached is Professor Erich Ippen's Final Technical Report for award number: W911NF-07-1-0630, Ultrafast Integrated Optical Signal Processing.

Questions of a technical nature should be addressed to:

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Sincerely yours,

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